In the Specification:

On page 1, please amend the paragraph beginning at line 5 as follows:

--The invention relates to a memory unit with at least two memory areas for storing data, first terminals for accessing data within the memory areas, and second terminals for accessing data within the memory [[area]] areas.--

On page 4, please amend the paragraph beginning at line 15 as follows:

--The data bus width may be 2^N, with N an integer. For instance data bus bandwidths of 8, 16, 32, 64, ... bit are supported. No particular bus protocol is necessary. The inventive memory unit may support ~~signal~~ single data rate (SDR) as well as double data rate (DDR) protocol, or any other protocol for control, address and/or data bus.--